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# Novel Configuration of Multilevel Inverter by Reduction in DC Sources

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**Abstract** – Inverters are widely employed in numerous contexts, including both home and industrial settings globally. Nevertheless, large harmonics in the inverter's output cause problems for ordinary inverters. Because of these benefits, multilayer inverters are becoming more and more common and are utilised in place of regular inverters. Many configurations are in place, but more DC sources are needed for them. This research study introduces a novel configuration of multilayer topology with fewer dc sources. The primary goal of this work is to suggest a unique topology with fewer dc-sources than the multilevel inverter design that is already in use. In this research, a novel technique called new pulse width modulation (NPWM) is devised to generate pulses for switches that are utilized in the suggested multilevel inverter arrangement. This document also presents the suggested inverter's detailed operation. This study develops a Hardware-in-the-Loop (HIL) system using OPAL-RT modules.

***Keywords*** – Multilevel Inverter, Reduced voltage Sources, pulse width modulation (PWM) technique.

## 1. INTRODUCTION

Using of power electronic devices is going rapidly day by day. Among many devices designed with the help of power electronic switches, inverter is mostly used to fulfil many objectives. Normal inverters produces only square wave type output where multilevel inverters can able to produce output near to sinusoidal with fewer harmonics. Many scholars implemented many configurations of multilevel inverters. Recently few configurations are developed with less number of switches. However, till more number of dc- sources in multilevel inverters are required.

More number of dc sources suffering from many issues. Hence a new configuration must be developed which consists of less number of dc source a well as switches. Hence this kind of configuration can be used in renewable energy sources models, electric vehicles, medium power drives etc. Applications of multilevel converters are implemented by many scholars recently where few of them presented here. A novel control of multilevel inverter is implemented by authors in [1] and also the importance of multilevel inverter. Authors in [2] developed a controller on multilevel inverter for the application of electric vehicle. A novel controller is implemented in a distribution system to integrate multiple renewable energy sources by authors in [3]. A MPPT algorithm is implemented for a power supply system powered from PV by authors in [4]. Various strategies, including capacitor placement and distributed generation (DG) integration, have been explored to enhance system efficiency [5]. The revised multilevel inverter architecture decreases the quantity of DC sources by using two sources in fundamental units for both symmetrical and asymmetrical configurations, resulting in fewer components, less power loss, and improved inverter efficiency relative to contemporary systems [6].

Voltage dip mitigation in distribution systems can be effectively achieved through the implementation of Distribution Static Synchronous Compensators (D-STATCOM). This technology enhances power quality by providing reactive power support, thereby stabilizing voltage levels and reducing losses in the system [7]. The suggested multilevel inverter design employs a single-phase H-bridge module with sub-switch technology, markedly decreasing the number of necessary DC sources while attaining 29 voltage levels, hence enhancing efficiency, diminishing complexity, and lowering total costs [8]. The new technique for cascaded H-bridge multilevel inverters (CHB-MLI) minimizes switch losses and increases

efficiency by choosing voltage levels with changeable DC sources in the best possible way. This improves output voltage quality and lowers total harmonic distortion (THD) [9-10]. The suggested multilevel inverter design decreases the quantity of DC sources by using capacitors for voltage division, so substantially reducing the number of switches and sources relative to earlier designs, hence improving efficiency and performance in single-phase applications [11-12]. The suggested multilayer inverter design improves voltage levels by integrating one additional switch, enabling two more output levels without augmenting the number of DC sources. This yields a more efficient setup with a reduced number of switches relative to conventional systems [13]. The suggested multilayer inverter design improves voltage levels by integrating one additional switch, enabling two more output levels without augmenting the number of DC sources. This yields a more efficient setup with a reduced number of switches relative to conventional systems [14]. The suggested sub-multilevel inverter configuration decreases the quantity of DC voltage sources while preserving elevated output levels. It employs an innovative submodule architecture that incorporates fewer power electronic components, hence improving efficiency and reducing conduction and switching losses [15]. The suggested multilayer inverter configuration minimizes the quantity of dc-link sources while attaining 9 to 17 output voltage levels. This topology improves efficiency by reducing the number of switches and lowering voltage needs relative to current multilayer inverter systems [16]. The paper introduces a multi-level symmetric inverter design that eliminates DC sources and switching devices, lowering voltage drop (Vstress) and Total Harmonic Distortion (THD) and improving efficiency [17]. This multilayer inverter layout eliminates switches and allows symmetrical and asymmetrical operation [18].A novel method of DC-DC converter proposed in [19-20].

This paper includes new configuration with a less numbers of components as well as dc sources. A new method for triggering the switches in the novel configuration is called new pulse width modulation, or NPWM. A seven level inverter only needs three carrier waves to produce three switching pulses for gating signals. The proposed configuration of a 7 level inverter required only eight numbers of switches. Hence, a modified digital pulse width modulation method is developed to fire the signals in proposed configuration.

Sections below are where the remainder of the paper is organised. Compressed with the suggested inverter setup is Section II. Section III provides a detailed explanation of the suggested configuration's operation. In Section IV, a new digital PWM approach is given. In Section-V, the findings are clarified and addressed. Section VI condenses the conclusion. An index of references is given at the conclusion of the document..

## II. PROPOSED TOPOLOGY

Fig. 1 shows the suggested topology of a 7 level inverter, which requires just 8 switches and 3 power sources. In this design, three voltage sources for each VDC/3 have been taken into consideration. On the load side, a single H-Bridge is utilised by connecting four switches, which are utilised to convert DC to AC. A pattern is constructed that is listed in Table 1 in order to turn on the devices. By using the switches in accordance with Table 1, the voltage levels of 0, VDC/3, VDC, 2VDC/3, -VDC/3, –VDC, and -2VDC/3 can be obtained.

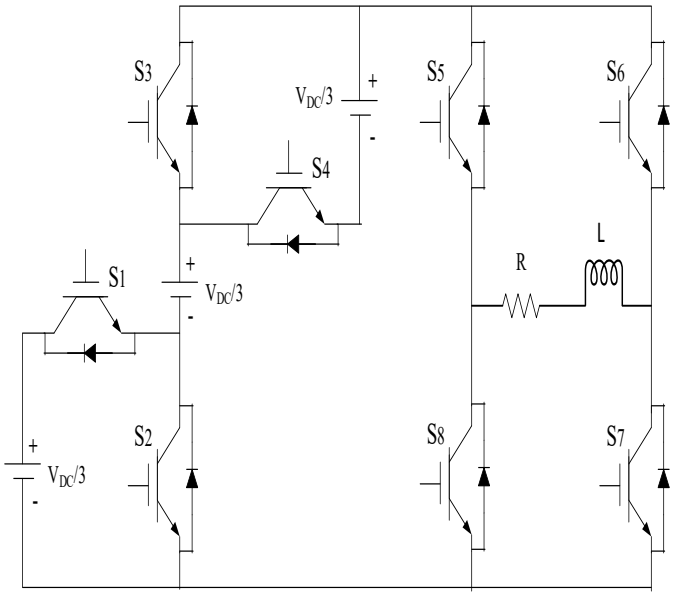


Fig. 1: Proposed topology of a 7 level inverter.

Table-1: Pattern for pulses.

| Voltage level. | Sequence of pulses. | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| $3V_{DC}$ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $2V_{DC}$ | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| $V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| $-V_{DC}$ | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $-2V_{DC}$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $-3V_{DC}$ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

## III. CIRCUIT OPERATION

This section presents the suggested topology's circuit operation. The diagrams below illustrate the path taken by current through switches at various stages.

Fig. 2 depicts the current flow for zero voltage, or zero level. There will be zero voltage across the load if switched ON both switches $S_5$ and $S_6$.

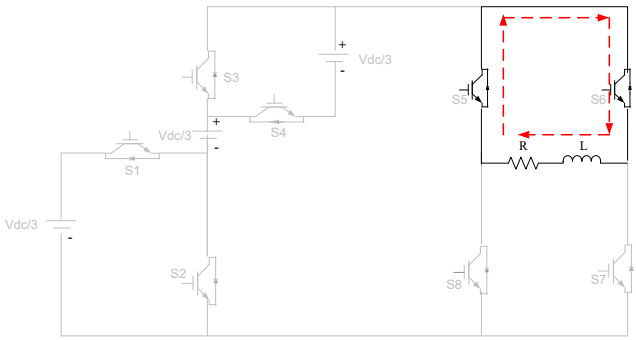


Fig. 3.Current path of zero voltage.

When switches $S_7$, $S_2$, $S_3$,& $S_5$are ON, $V_{DC}/3$ level for voltage will be appear at the load as shown in Fig. 3.

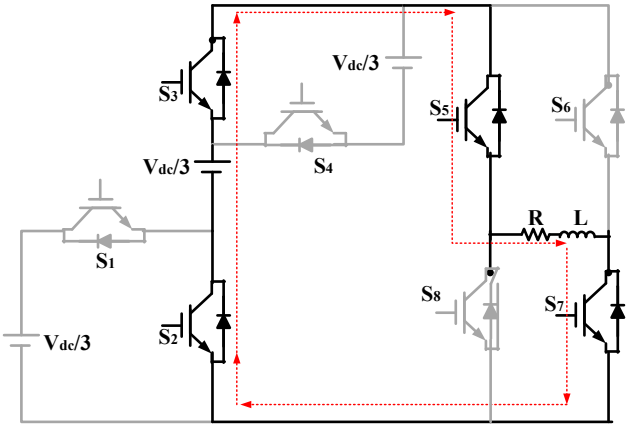


Fig. 3: Voltage level for '$V_{DC}/3$'.

In order to achieve the level of $2V_{DC}/3$ voltage, switches $S_7$, $S_2$, $S_4$,& $S_5$are ON as the current path depicted in Fig.4.Fig. 5depicted the current path for the level $V_{DC}$ when switches $S_1$, $S_4$, $S_5$, & $S_7$need to be ON.The voltage level for the voltage '$-V_{DC}/3$'isachieved by ON state of switches $S_2$, $S_3$, $S_6$, and $S_8$andshown in Fig. 6.

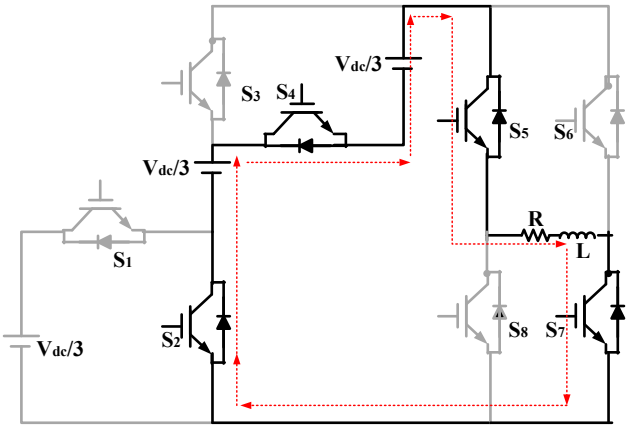


Fig. 4: Level '$2V_{DC}/3$' of voltage.

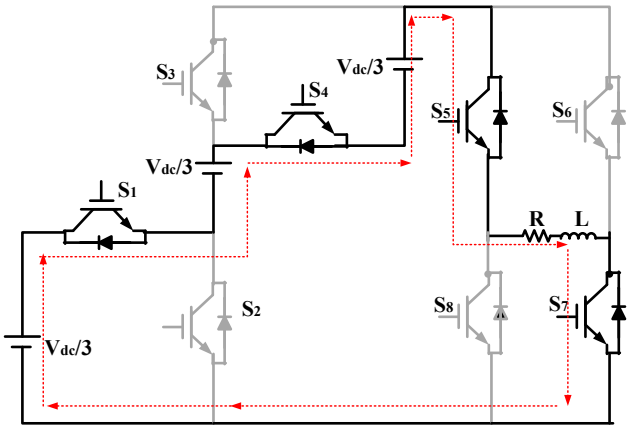


Fig. 5: Voltage level '$V_{DC}$'.

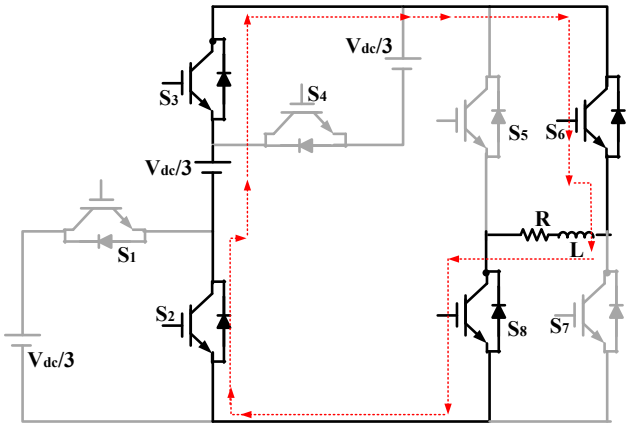


Fig. 6: Voltage level for '$-V_{DC}/3$'.

The current path of the Fig. 8 is depicted to obtain the level '$-2V_{DC}/3$' by switching ON switches $S_2$, $S_4$, $S_6$, and $S_8$.

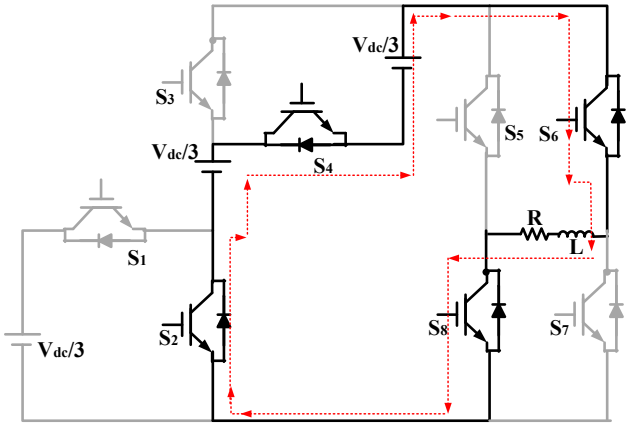


Fig. 7: Level of '$-2V_{DC}/3$'.

In order to obtain '$-V_{DC}$' level, the switching sequence $S_1$, $S_4$, $S_6$, and $S_8$must be ON as shown inFig.8.

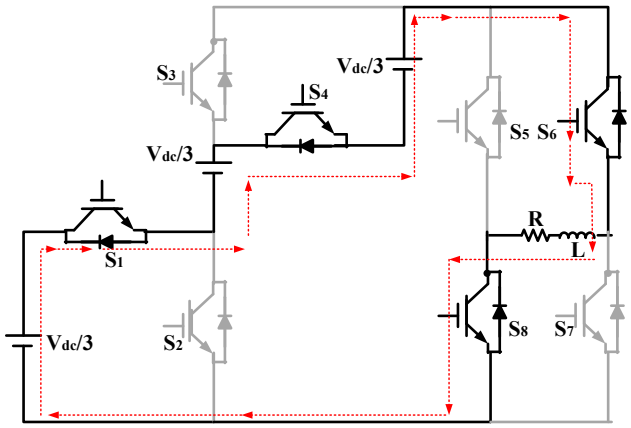


Fig. 8:'-$V_{DC}$'level of voltage.

## IV. DIGITAL PWM METHOD

In order to obtain the 7 level output with a proper sequence of switching pulses as mentioned in above, the switching stages are listed in table-2. A digital PWM using logic gates is considered in this paper to produce proper switching sequence. There are three carrier signals of A, B, C considered. The proper generation of pulses is depicted in Fig. 9.

Table-2: Switching notation.

| Switch | Pulse. |
|---|---|
| $S_1$ | C |
| $S_2$ | $A\overline{C}$ |
| $S_3$ | $A\overline{B}$ |
| $S_4$ | B |
| $S_5$ | $\overline{A}\overline{D}+D$ |
| $S_6$ | $\overline{D}+\overline{A}D$ |
| $S_7$ | AD |
| $S_8$ | $A\overline{D}$ |

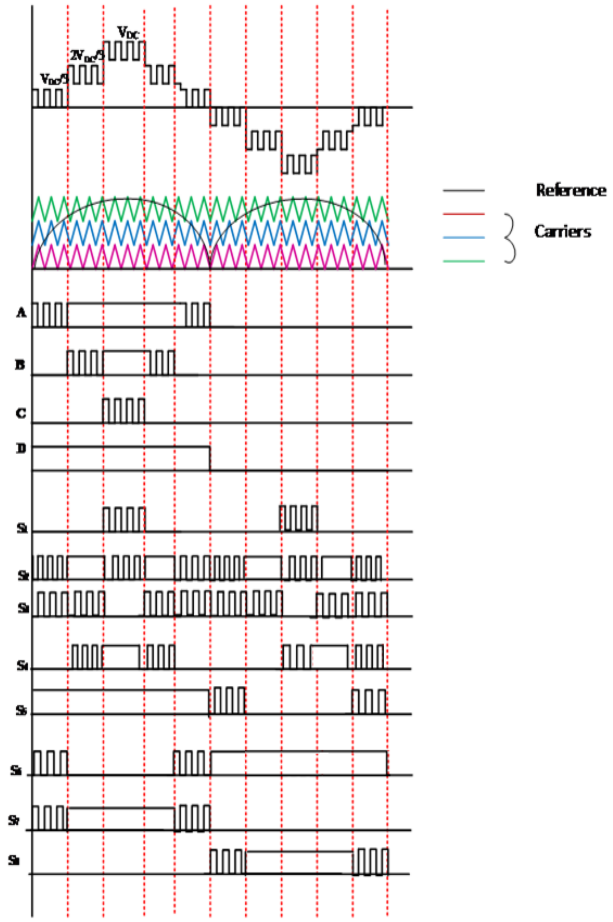


Fig. 9: Digital .PWM process.

## V. RESULTS AND DISCUSSIONS

In this work, real-time simulators (RTS) are used to enhance the system's performance under various conditions. In the lab, RTS modules such as OPAL-RT devices are used for HIL configuration. To get hands-on experience testing proposed sophisticated controllers, HIL is developed using two OPAL-RT modules.

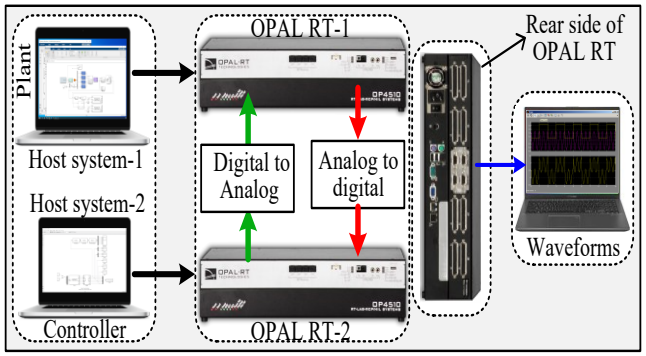


Fig. 10: HIL setup for results.

Only resistive type loads are taken into consideration in order to clearly explain data about a seven level representation. Figure 11 displays the phase voltage along with the average sinusoidal wave. Similarly, Fig. 12 shows

line to line voltage. Figures 13 and 14 display the corresponding THD of current and voltage, respectively..

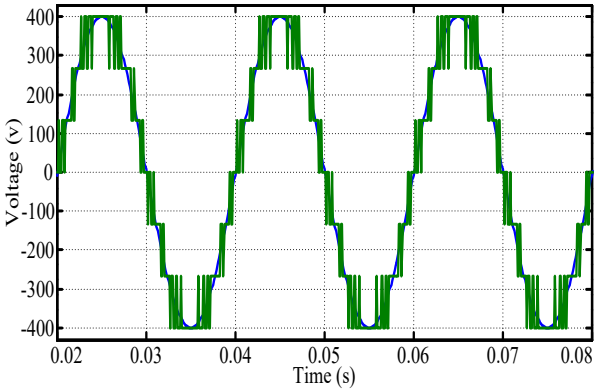


Fig. 11: Phase voltage of an inverter with seven levels.

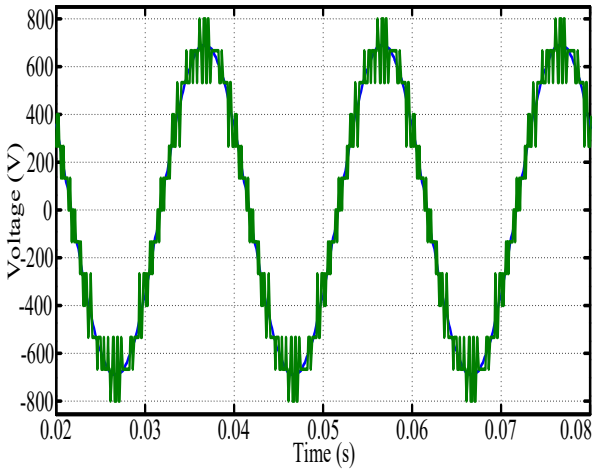


Fig. 12: line to line voltage of a seven level inverter.

In general loads are incorporated at load bus and the LC filter will be connected between inverter and load bus, hence the harmonics will be further reduced.

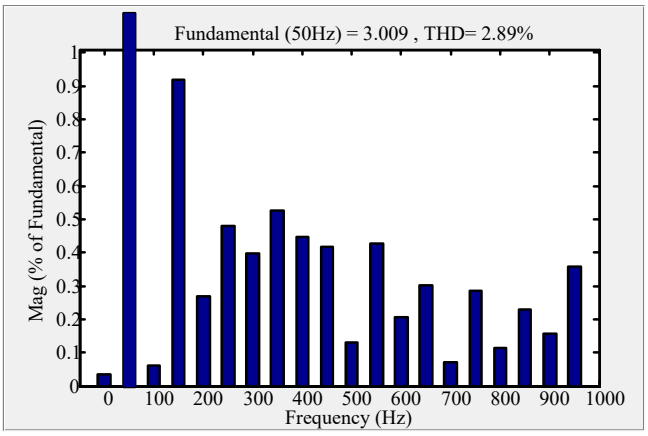


Fig. 13: THD of line current.

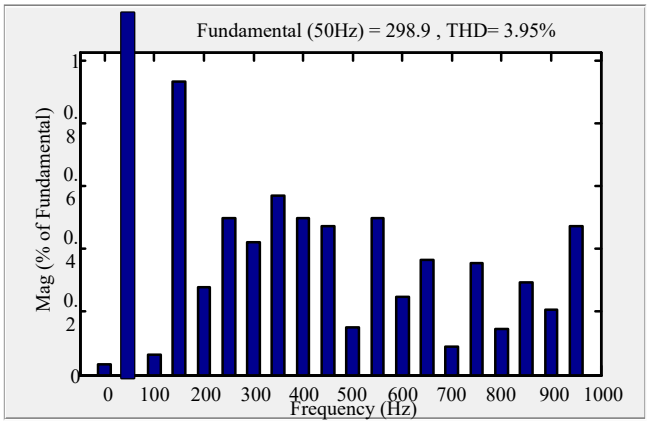


Fig. 14: THD of a line voltage.

## VI. CONCLUSIONS

Using fewer power sources, this study provides a seven-level inverter architecture. To generate a suitable pulse sequence, a new configuration is created and simulated using the DPWM technique. A resistive type load is considered when analysing the data at the load bus. The average sinusoidal waveform of the load bus's phase and line-to-line voltages is presented beside them for better understanding. The THD spectrum for a line-to-line voltage and current is shown in this paper. HIL offers useful results and is established by the use of OPAL-RT devices. The recommended configuration is commonly employed to incorporate the inverter into any multilayer inverters that are presently in operation.

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